

02/24/00  
jc772 U.S. PTO

02-25-00

A/PD-11

Express Mail No: EL480562428US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Tsutomu Ishikawa et al.

jc525 U.S. PTO  
02/24/00  
09/552685

For: SEMICONDUCTOR INTEGRATED CIRCUIT HAVING PADS WITH LESS  
INPUT SIGNAL ATTENUATION

LETTER

The Commissioner of Patents  
and Trademarks  
Washington, D.C. 20231

Dear Sir:

The attached application for U.S. Patent is being filed under the provisions of Rule 1.53 of the Rules of Practice in Patent and Trademark cases. Accordingly, we are enclosing the following documents at this time:

- (a) Specification including abstract 16 pages; 18 Claims; and
- (b) Drawings (7 sheets)

The filing fee, Declaration and Assignment documents will be submitted later under the provisions of 37 CFR 1.53.

Please be advised that the inventor of the invention disclosed in the attached specification and claims is: Tsutomu Ishikawa and Hiroshi Kojima.

Please also be advised that the undersigned has been authorized to file this application on his behalf.

"Express Mail" mailing label number EL480562428US  
Date of Deposit 2-24-00  
I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.  
Sandra E. McLaughlin  
(Typed or printed name of person mailing paper or fee)  
Sandra E. McLaughlin  
(Signature of person mailing paper or fee)

If there are any additional charges with respect to this patent application or otherwise, please charge them to Deposit Account No. 06-1130 maintained by Applicants' attorney.

Please send correspondence to:

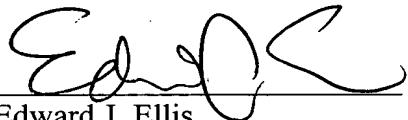
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Respectfully submitted,

Tsutomu Ishikawa et al.

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